1.3 GHz Singled Ended Amplifier Design

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Design Requirements

Focusing on maximizing the gain and minimizing return loss.

+11dB Single-Ended Transistor Amplifier

Center frequency of 1.3 GHz

VSWR = 2:1



Circuit



Bias Transmission Line





LineCalc/line	calc.lcs							- 0		
e Simulation	Options Help									
) 📁 🗖										
Component										
ype MLIN	▼ ID M	ILIN: MLIN	DEFAULT	•						
Substrate Parameters				Physical W	3.022290	mm	•			
Fr	4 400	N/A	~ ^	L	31.663400	mm	•			
Mur	1.000	N/A	-			N/A	Ψ.			
н	1.600	mm	•			N/A	Υ.			
Hu	1e+33 mm 🔻			Synthesize Analyze						
т	0.035	mm	•			V		Calculated Results		
Cond	1.0E+50	N/A	~	Electrical				K_Eff = 3.315 A DB = 0.123		
TapD	0.020	NL/A	• •	ZO	50.000	Ohm	•	SkinDepth = 0.000		
Component Parameters			E_Eff	90.000	deg	•				
Freq	Freq 1.300 GHz		•			N/A	v			
Wall1		mil	•			N/A	Y			

Values are consistent



SNP File from VNA



Calculations

- $D = S_{11}S_{22} S_{12}S_{21}$ $K = \frac{1 |S_{11}|^2 |S_{22}|^2 + |D|^2}{2|S_{12}S_{21}|}$ $B_1 = 1 + |S_{11}|^2 |D|^2 |S_{22}|^2$ $C_1 = S_{11} DS_{22}^*$ $B_2 = 1 + |S_{22}|^2 |D|^2 |S_{11}|^2$ $C_2 = S_{22} DS_{11}^*$
- A 2-port is unconditionally stable if:

K > 1 and |D| < 1

$$\Gamma_{ms} = \frac{B_1 \pm \sqrt{B_1^2 - 4|C_1|^2}}{2C_1} \quad \Gamma_{ml} = \frac{B_2 \pm \sqrt{B_2^2 - 4|C_2|^2}}{2C_2}$$

Available Power Gain:

$$G_A \equiv \frac{\mathcal{P}_{avo}}{\mathcal{P}_{avs}} = \frac{|S_{21}|^2 \left(1 - |\Gamma_S|^2\right)}{(1 - |S_{22}|^2) + |\Gamma_S|^2 (|S_{11}|^2 - |D|^2) - 2Re(\Gamma_S C_1)}$$

Transducer Power Gain:

$$G_T \equiv \frac{P_{\text{out}}}{P_{\text{avs}}} = \frac{|S_{21}|^2 \left(1 - |\Gamma_S|^2\right) \left(1 - |\Gamma_L|^2\right)}{|(1 - S_{11}\Gamma_S)(1 - S_{22}\Gamma_L) - S_{12}S_{21}\Gamma_L\Gamma_S|^2}$$

$$Z_X = Z_o \frac{1 + \Gamma_X}{1 - \Gamma_X}$$

$$G_{A,max} = \left| \frac{S_{21}}{S_{12}} [K \pm \sqrt{K^2 - 1}] \right|$$



1 -	clear	Workspace			
2 -	close				
3	<pre>%%% Matching Network Design %%%</pre>	Name 🔺	Value		
4 -	<pre>phasor = @(mag,ang) mag*cosd(ang)+1j*mag*sind(an S11 = mbasar(0,65,50,76);</pre>				
5 - 6 -	SII = phasor(0.03, 50.70); SI2 = phasor(0.083 - 11.2399);	🛨 B1	1.3719		
7 -	S12 = phasor(0.003, -11.2335); S21 = phasor(2.79, -6.00);	H B2	0.5788		
8 -	S22 = phasor(0.161,-102.937);		0.4160 . 0.4700:		
9					0.4108 + 0.47881
10	%%%%Gains and others	🕂 C2	-0.1006 - 0.0779i		
11 -	D = 0.157; %From ADS simulation	H D	0 1570		
12 -	<pre>K = 1.132; %From ADS simulation</pre>		0.570		
13		GA GA	9.5734		
14 -	$B1 = 1 + abs(S11)^2 - D^2 - abs(S22)^2;$ $C1 = S11 - Dteopt(S22);$	🛨 Gmax	20.2193		
16 -	$CI = SII = D^{\circ}CONJ(S22);$ $B2 = 1 \pm abs(S22)^{2} = D^{2} = abs(S11)^{2}.$	GT	13 7703		
17 -	$C_2 = S_{22} - D^* conj(S_{11})$:		13.1703		
18	; (; /			🛨 GuT	13.4797
19 -	Rs = (Bl - sqrt(Bl^2 - 4*abs(Cl)^2))/(2*Cl);	%Reflection of the source		К	1.1320
20 -	<pre>R1 = (B2 - sqrt(B2² - 4*abs(C2)²))/(2*C2);</pre>	<pre>%Reflection of the load</pre>		nhacor.	@(mag ang)mag*cos
21	-			phason	@(mag,ang)mag.cos
22 -	Zs = 50 * (1+Rs)/(1-Rs)	%Impedance of the source side		📩 RI	-0.1831 + 0.1418i
23 -	Z1 = 50 * (1+R1)/(1-R1)	%Impedance of the load side		🕂 Rs	0.4407 - 0.5062i
25 -	GA 🚆 [(abs(S21)^2)*(1-abs(R1)^2)]/[(1-(abs(S22)^	H S11	0.4112 + 0.5034i		
26	-			F \$12	0.0814 - 0.0162i
27 -	GT 👖 [(abs(S21)^2)*(1-abs(Rs)^2)*(1-(abs(R1)^2))		0.0014 - 0.01021		
28		521	2.7747 - 0.2916		
30	Gui 🚆 [(1-(abs(Rs))^2)/abs(1-Sii*Rs)^2]*(abs(S21	🛨 S22	-0.0360 - 0.1569i		
31 -	Gmax 🚍 abs((S21/S12)*[K - sqrt(K^2-1)])	E ZI	33.3247 + 9.9844i		
32				Zs	48,2884 - 88,9500i
33					

Matching networks



Matching network cont.



1. Calculate Z_S and Z_L for MN



2. Smith chart tool to find TX line length



3. Simulate the 2-port power gain

Matching network cont.



Matching network cont.



Empirical Result; Return Loss

Initial attempt



Stop 3 GHz Cor

Meas Stop E

Empirical Result; Return Loss

Initial attempt





Empirical Result; Gain

Initial attempt



Empirical Result; Circuit



Empirical Result; Gain

Final attempt



Empirical Result ; Return Loss

Final attempt



Conclusion

Challenges Faced

- SMA broke during testing
- MATLAB results vs SNP results
- Inaccurate placement of Stubs

- Solder and Board Placement
- Check for Typos (Interpret as Output Impedance)
- Consistent measurements

• Tuning ADS Values

What happens if the frequency is increased?